AMENDMENTS TO THE CLAIMS

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED

REVISION TO 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

one or more logic circuits configured to provide logical operation, wherein said one or more logic circuits comprise (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable ~~logic~~ elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

2. (ORIGINAL) The apparatus according to claim 1, wherein said one or more logic circuits comprise variable width logic circuits.

3. (ORIGINAL) The apparatus according to claim 2, wherein a width of each of said one or more logic circuits is determined in response to one or more input signals.

4. (ORIGINAL) The apparatus according to claim 1, wherein each of said one or more logic circuits is configured to

receive a first one or more inputs, wherein said first one or more inputs comprise multi-bit or single-bit signals in a serial or a parallel configuration.

5. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein one or more of said ~~logic circuits~~ non-programmable hard wired blocks comprises a hard wired multiplier.

6. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein one or more of said non-programmable hard wired blocks ~~logic circuits~~ are configured to perform ~~a~~ cyclic redundancy check (CRC) functions.

7. (PREVIOUSLY AMENDED) The apparatus according to claim 1, wherein one or more of said logic circuits is configured to present an output.

8. (PREVIOUSLY AMENDED) The apparatus according to claim 7, wherein each of said one or more outputs comprise intermediate signals.

9. (ORIGINAL) The apparatus according to claim 7, further comprising:

an adder circuit configured to receive said one or more outputs.

10. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said routable interconnect circuit is configured to route signals to/from one or more of said non-programmable ~~elements~~ hard wired blocks.

11. (PREVIOUSLY AMENDED) The apparatus according to claim 10, further comprising a number of registers configured to increase a throughput of said one or more logic circuits.

12. (ORIGINAL) The apparatus according to claim 1, wherein each of said one or more logic circuits comprise an input portion configured to store one or more input signals.

13. (ORIGINAL) The apparatus according to claim 12, wherein each of said one or more logic circuits comprises an output portion configured to store an output.

15. (CURRENTLY AMENDED) An apparatus comprising:

means for receiving one or more input signals; and

means for performing logical operation on said input signals using (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable ~~logic~~ elements within a programmable logic device (PLD), wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

16. (CURRENTLY AMENDED) A method for computing in a programmable logic device (PLD) comprising the steps of:

(A) receiving one or more input signals;

(B) performing logical operation on said one or more input signals with (i) programmable logic elements and (ii) non-programmable hard wired blocks having no programmable ~~logic~~ elements within said programmable logic device, wherein said programmable logic elements are (i) configurable between two or more different logical functions and (ii) connectable by a routable interconnect circuit.

17. (PREVIOUSLY AMENDED) The method according to claim 16, further comprising the step of:

(C) generating one or more output signals.

18. (CURRENTLY AMENDED) The method according to claim 16, wherein step (B) further comprises:

multiplying said one or more input signals with one or more of said hard wired blocks.

19. (PREVIOUSLY AMENDED) The method according to claim 17, wherein step (B) further comprises:

receiving said one or more outputs and adding said one or more outputs.

20. (PREVIOUSLY AMENDED) The method according to claim 17, wherein step (C) further comprises:

routing said one or more outputs with said routable interconnect circuit.

21. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said non-programmable hard wired blocks ~~elements~~ comprise dedicated logic having a ~~specific functionality~~ fixed implementation of a given functional block on silicon.

22. (PREVIOUSLY NEW) The apparatus according to claim 1, wherein said programmable elements comprise configurable macrocells.

23. (CURRENTLY AMENDED) The apparatus according to claim 1, further comprising:

one or more first registers configured to couple one or more input signals to said non-programmable ~~logic elements~~ hard wired blocks; and

one or more second registers configured to receive one or more output signals from said non-programmable ~~logic elements~~ hard wired blocks.

End

24. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said non-programmable ~~logic elements~~ hard wired blocks (i) comprise hard wired multipliers having a first width and (ii) are couplable to form one or more multipliers having a second width.